Stratos Optical
2.97G Video SFP Transceiver

Connectivity for
Business Critical Continuity

FEATURES

- SMPTE 424M/297M compliant
- SMPTE 292M/259M/297M compatible
- Based on industry standard SFP
- Keyed to support dual TX and RX options
- RoHS-6 compliant
- Handles pathological test matix pattern
- Internally Calibrated Digital Diagnostic Monitoring Interface
- 100Ω differential AC coupled CML Outputs
- Die Cast Metal Housing
- Hot pluggable

PRODUCT OVERVIEW

The SPLC-20-P-X-B optical Video Small Form Factor Pluggable (V_SFP) transceivers are high performance integrated duplex data links for bi-directional communication over single mode optical fiber. These transceivers are designed to transmit/receive data rates from 270Mbps to 2.97Gbps and are compatible with the following standards:

- SMPTE 424M/297M (1080p -- 2.97Gbps)
- SMPTE 292M/297M (HDTV -- 1.485Gbps)
- SMPTE 259M/297M (SDTV -- 270/360Mbps)

The Stratos Optical V_SFP transceiver is hot pluggable which allows a suitably designed enclosure to be changed from one type of external interface to another simply by plugging in a V_SFP having the alternative external interface. The SPLC-20-P-X-B operates using a single 3.3V supply.

This optoelectronic transceiver module is a Class 1 Laser product compliant with FDA Radiation Performance Standards, 21 CFR Subchapter J. This component is also Class 1 Laser compliant according to International Safety Standard IEC-825-1.

LONG WAVELENGTH LASER

The SPLC-20-P-X-B transmitter lasers are provided with an internal facing angle polished fiber stub. Standard single mode optical patch cord with Standard Polished Connector (SPC) is required.

LONG WAVELENGTH RECEIVER

The SPLC-20-P-X-B receiver subassemblies are provided with an internal facing angle polished fiber stub. Standard single mode optical patch cord with Standard Polished Connector (SPC) is required.

ORDERING INFORMATION

SPLC - 20 - P - X - B

RELEASE ACTUATOR
B = Bail Actuator

TRANSMITTER/RECEIVER TYPE
2 = 1310nm FP Tx / PIN Rx
2M = 1310nm DFB Tx / PIN Rx
2L = 1310nm DFB Tx / APD Rx*
3 = 1550nm DFB Tx / PIN Rx
3L = 1550nm DFB Tx / APD Rx*

COMMUNICATIONS PROTOCOL
P = SMPTE 424M/292M/259M/297M with Digital Diagnostics 270MBaud to 2.97GBaud

* Contact factory for availability

MODULE SPECIFICATIONS - ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	Tstg	-40	+85	°C	
Supply Voltage	$V_{CC}T$, $V_{CC}R$		6.0	V	VCC - ground
Data AC Voltage	Tx+, Tx-		2.6	Vpp	Differential
Data DC Voltage	Tx+, Tx-	-10	10	Vpk	V (Tx+ or Tx-) - ground

MODULE SPECIFICATION - RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Ambient Case Temperature	Tc	0		+70	°C	
Supply Voltage	$V_{DD}T$, $V_{DD}R$	+3.135	+3.3	+3.435	VDC	
Buad Rate	BRate	270		2.97	Mbps	270/360/1485/2970Mbps

ELECTRICAL SPECIFICATIONS

0ºC<Tc<+70ºC; +3.135<Vcc<+3.465V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current (SPLC-20-9D-2-B)	Icc		170	210	mA	Tc = 25°C, Vcc = +3.3 V
				300	mA	0°C<Tc<+70°C, +3.135 V< Vcc <+3.465V
Supply Current (SPLC-20-9D-2M-B)	Icc		170	210	mA	Tc = 25°C, Vcc = +3.3 V
				300	mA	0°C<Tc<+70°C, +3.135 V< Vcc <+3.465V
Supply Current (SPLC-20-9D-3-B)	Icc		170	210	mA	Tc = 25°C, Vcc = +3.3 V
				325	mA	0°C<Tc<+70°C, +3.135 V< Vcc <+3.465V
Surge Current	Isurge			30	mA	Surge above steady state value
TRANSMITTER						
CML/LVPECL Inputs (Differential)		300		1860	mVpp	AC coupled inputs
Input Impedance (Differential)	Zin	95	100	105	ohms	Rin > 100 kohms @ DC
Tx_DISABLE Input Voltage - High	ViH	2		3.45	V	
Tx_DISABLE Input Voltage - Low	ViL	0		0.8	V	
RECEIVER						
CML Outputs (Differential)		400	800	950	mVpp	AC Coupled Outputs
Total Jitter [Pk - Pk]	TJ			120	ps	Measured with Pathological Test Matrix Pattern @2970/1485/360/270Mbps (note 1)
				100	ps	Measured with Color Bar Test Signal @2970/1485/360/270Mbps (note 1)
Return Loss		15			dB	Worst case @ 10KHz to 3GHz
SCL, SDA	VoH	2.5		Vcc+0.3	V	
	VoL	0		0.5	V	

Note 1: Maximum Jitter is specified for single module point-to-point applications only. In cascaded configurations, where the receiver electrical output is directly interfaced with the transmitter electrical input of a separate module, accumulated jitter may result in CRC errors to occur during pathological pattern transmission. For error-free operation in such a situation, use of re-clocker device is recommended at the output of the receiver before interfacing to the inputs of the optical transmitter. This will ensure that the output jitter will not exceed the input jitter tolerance of the succeeding transmitter input.

SPLC-20-P-2-B OPTICAL SPECIFICATIONS (1310nm FP/PIN) **0ºC<Tc<+70ºC; +3.135<Vcc<+3.465V**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Link Distance (9.0µm Core Diameter SMF)		10	25		km	@ 2.97Gbps (note 2)
		20	35		km	@ 1.485Gbps (note 2)
		35	45		km	@ 270/360Mbps (note 2)
TRANSMITTER						
Optical Center Wavelength	λ	1290	1310	1330	nm	Tcase = +25ºC
Spectral Width	Δλ			2.5	nm	RMS
Optical Transmit Power	Popt	-6		-2	dBm	Average @ 1310nm
Extinction Ratio	ER	7			dBm	P1/P0
Relative Intensity Noise	RIN			-117	dB/Hz	
Total Jitter [Pk - Pk]	TJ			120		Measured with Pathological Test Matrix Pattern @2970/1485/360/270Mbps
				100	ps	Measured with Color Bar Test Signal @2970/1485/360/270Mbps
Output Rise Time	t_R			100	ps	20%-80%; Measured unfiltered @2970/1485/360/270Mbps
Output Fall Time	t_F			120	ps	
RECEIVER						
Optical Input Wavelength	λ	1270		1610	nm	
Optical Input Power with Pathological Test Matrix Pattern (note 3)	Pr	-20		-3		@ 2.97Gbps
		-20		-3		@ 1.485Gbps
		-23		-3	dBm	@ 270/360Mbps
Optical Input Power with Color Bar Test Signal (note 3)	Pr	-21		-3		@ 2.97Gbps
		-21		-3		@ 1.485Gbps
		-24		-3	dBm	@ 270/360Mbps
Optical Return Loss	ORL	29			dB	
RX_LOS --- Asserted	Pa	-29			dBm	No Signal Pins Designated for RX_LOS. Assert/Deassert Levels can be Monitored via Digital Diagnostics Interface.
RX_LOS --- Deasserted	Pd			-20	dBm	
RX_LOS --- Hysteresis	Pa - Pd		1.5	5	dB	

Note 2: The specified minimum link distances are based on IEEE link budget models. Assumes minimum transmitter output power and extinction ratio and worst case receiver sensivitity with pathological test matrix pattern.

Note 3: Minimum receiver input power is defined for line BER < 1 x 10^{-12}. When connecting SPLC-20-P-2-B transmitter and receiver module using 2-3m fiber patch cord, the user shall place a 1dB in-line attenuation to prevent receiver overload.

SPLC-20-P-2M-B OPTICAL SPECIFICATIONS (1310nm DFB/PIN) **0ºC<Tc<+70ºC; +3.135<Vcc<+3.465V**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Link Distance (9.0µm Core Diameter SMF)		35	50		km	@2.97Gbps (note 2)
		40	55		km	@1.485Gbps (note 2)
		45	60		km	@270/360Mbps (note 2)
TRANSMITTER						
Optical Center Wavelength	λ	1300	1310	1320	nm	Tcase = +25ºC
		1280		1335		Tcase = 0ºC<Tc<+70ºC
Side Mode Suppression Ratio	SMSR	30	40		dB	
Optical Transmit Power	Popt	0		+3	dBm	Average @ 1310nm
Extinction Ratio	ER	7			dBm	P1/P0
Relative Intensity Noise	RIN			-117	dB/Hz	
Total Jitter [Pk - Pk]	TJ			120	ps	Measured with Pathological Test Matrix Pattern @2970/1485/360/270Mbps
				100	ps	Measured with Pathological Pattern Test Signal @2970/1485/360/270Mbps
Output Rise Time	t_R			100	ps	20%-80%; Measured unfiltered @2970/1485/360/270Mbps
Output Fall Time	t_F			120	ns	
RECEIVER						
Optical Input Wavelength	λ	1270		1620	nm	
Optical Input Power with Pathological Test Matrix Pattern (note 3)	Pr	-20		-3	dBm	@ 2.97Gbps
		-20		-3	dBm	@ 1.485Gbps
		-23		-3	dBm	@ 270/360Mbps
Optical Input Power with Color Bar Test Signal (Note 3)	Pr	-21		-3	dBm	@ 2.97Gbps
		-21		-3	dBm	@ 1.485Gbps
		-24		-3	dBm	@ 270/360Mbps
Optical Return Loss	ORL	29			dB	
RX_LOS --- Asserted	Pa	-29			dBm	No Signal Pins Designated for RX_LOS. Assert/Deassert Levels can be Monitored via Digital Diagnostics Interface.
RX_LOS -- De-sserted				-20	dBm	
RX_LOS --- Hysteresis	Pa - Pd		1.5	5	dB	

Note 2: The specified minimum link distances are based on IEEE link budget models. Assumes minimum transmitter output power and extinction ratio and worst case receiver sensivitity with pathological test matrix pattern.

Note 3: Minimum receiver input power is defined for line BER < 1 x 10^{-12}. When connecting SPLC-20-P-2M-B transmitter and receiver module using 2-3m fiber patch cord, the user shall place a 6dB in-line attenuation to prevent receiver overload.

SPLC-20-P-3-B OPTICAL SPECIFICATIONS (1550nm DFB/PIN) **0ºC<Tc<+70ºC; +3.135<Vcc<+3.465V**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Link Distance (9.0µm Core Diameter SMF)		50	55		km	@ 2.97Gbps (note 2)
		60	75		km	@ 1.485Gbps (note 2)
		75	100		km	@ 270/360Mbps (note 2)
TRANSMITTER						
Optical Center Wavelength	λ	1540	1550	1565	nm	Tcase = +25ºC
		1480		1580		Tcase = 0ºC<Tc<+70ºC
Side Mode Suppression Ratio	SMSR	30	40		dB	
Optical Transmit Power	Popt	0		+3	dBm	Average @ 1550nm
Extinction Ratio	ER	7			dBm	P1/P0
Relative Intensity Noise	RIN			-117	dB/Hz	
Total Jitter [Pk - Pk]	TJ			120	ps	Measured with Pathological Test Matrix Pattern @2970/1485/360/270Mbps
				100	ps	Measured with Color Bar Test Signal @2970/1485/360/270Mbps.
Output Rise Time	t_R			100	ps	20%-80%; Measured unfiltered @2970/1485/360/270Mbps
Output Fall Time	t_F			120	ns	
RECEIVER						
Optical Input Wavelength	λ	1270		1620	nm	
Optical Input Power with Pathological Test Matrix Pattern (note 3)	Pr	-20		-3	dBm	@ 2.97Gbps
		-20		-3	dBm	@ 1.485Gbps
		-23		-3	dBm	@ 270/360Mbps
Optical Input Power with Color Bar Test Signal (Note 3)	Pr	-21		-3	dBm	@ 2.97Gbps
		-21		-3	dBm	@ 1.485Gbps
		-24		-3	dBm	@ 270/360Mbps
Optical Return Loss	ORL	29			dB	
RX_LOS --- Asserted	Pa	-29			dBm	No Signal Pins Designated for RX_LOS. Assert/Deassert Levels can be Monitored via Digital Diagnostics Interface.
RX_LOS -- De-sserted				-20	dBm	
RX_LOS --- Hysteresis	Pa - Pd		1.5	5	dB	

Note 2: The specified minimum link distances are based on IEEE link budget models. Assumes minimum transmitter output power and extinction ratio and worst case receiver sensivitity with pathological test matrix pattern.

Note 3: Minimum receiver input power is defined for line BER < 1 x 10^{-12}. When connecting SPLC-20-P-3-B transmitter and receiver module using 2-3m fiber patch cord, the user shall place a 6dB in-line attenuation to prevent receiver overload.

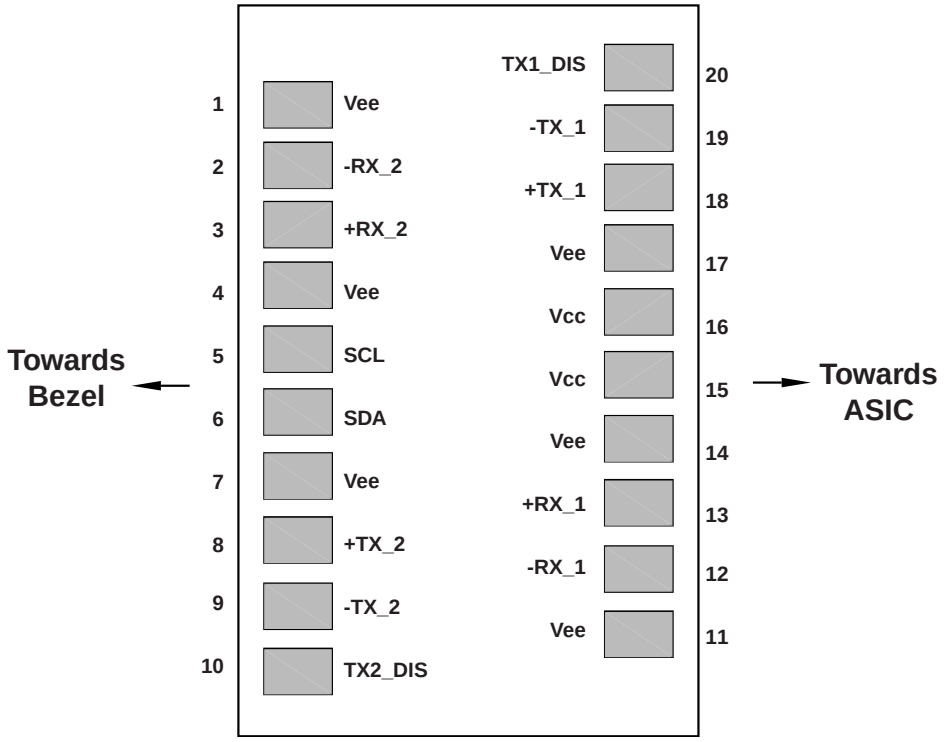


Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names

PIN NO.	NAME	FUNCTION	PLUG SEQ.	NOTES
PIN 1	Vee	Signal Ground	1	
PIN 2	-RX_2	Inverted Received Data out (2)	3	Note 4
PIN 3	+RX_2	Non-Inverted Received Data out (2)	3	Note 4
PIN 4	Vee	Signal Ground	1	
PIN 5	SCL	Serial Clock	3	
PIN 6	SDA	Serial Data	3	
PIN 7	Vee	Signal Ground	1	
PIN 8	+TX_2	Non-inverted Data In (2)	3	Note 5
PIN 9	-TX_2	Inverted Data In (2)	3	Note 5
PIN 10	TX2_DIS	Transmitter Disable (2)	3	Note 6
PIN 11	Vee	Signal Ground	1	
PIN 12	-RX_1	Inverted Received Data out	3	Note 7
PIN 13	+RX_1	Non-Inverted Received Data out	3	Note 7
PIN 14	Vee	Signal Ground	1	
PIN 15	Vcc	Power Supply	2	+3.3V ±5%, Note 8
PIN 16	Vcc	Power Supply	2	+3.3V ±5%, Note 8
PIN 17	Vee	Signal Ground	1	
PIN 18	+TX_1	Non-inverted Data In	3	Note 9
PIN 19	-TX_1	Inverted Data In	3	Note 9
PIN 20	TX1_DIS	Transmitter Disable	3	Note 10: Module Disables on high or open

Plug Sequence: Pin engagement sequence during hot plugging.

NOTES:
(4) ± RX_2: Floating; Not internally connected

(5) ± TX_2: Floating; Not internally connected

(6) TX2_DIS: Floating; Not Internally Connected.

(7) ± RX_1: These are the differential receiver CML level outputs. They are AC coupled 100ohm differential lines which should be terminated with 100ohm (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 1200mV differential (200-600mV single ended) when properly terminated. Refer to figure 2 for recommended receive data lines terminations.

(8) Vcc: are the receiver and transmitter power supplies. They are defined as 3.3V±5% at the V_SFP connector pin. Recommended host board power supply filtering is shown in figure 3. When the recommended supply filtering network is used, hot plugging of the V_SFP module will result in an inrush current of no more than 30mA greater than the steady state value.

(9) ± TX_1: are the differential transmitter inputs. They are AC coupled differential lines with 100ohm differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swing of 300 - 1860 mV differential (150-930mV single ended).

(10) TX1_DIS: is an input that is used to shut down the transmitter optical output when laser fault condition (internally latched) occurs. . It is internally pulled up with a 4.7K - 10K ohm resistor. The states are:

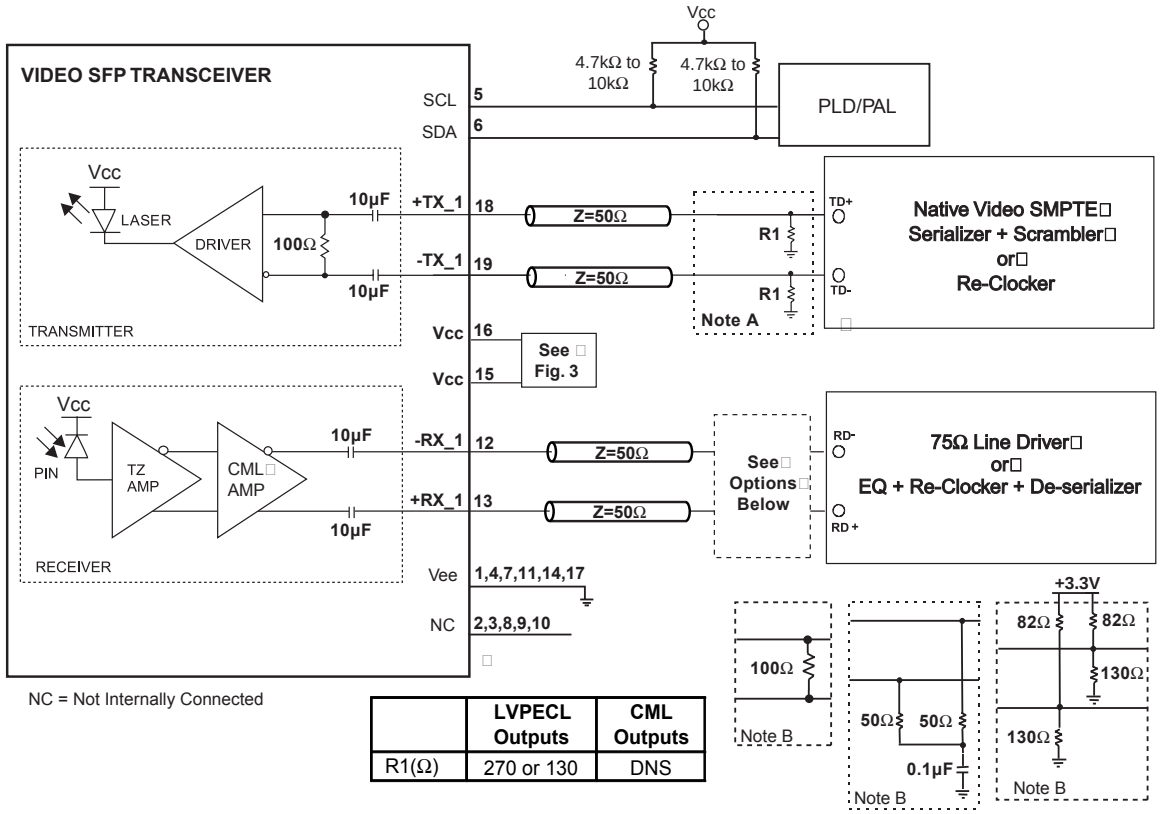
Low (0 - 0.8V):	Transmitter ON
(>0.8, <2.0V):	Undefined
High (2.0 - 3.465V):	Transmitter Disabled
Open:	Transmitter Disabled

TERMINATION CIRCUITS

Inputs to the SPLC-20-P-X-B transmitter are AC coupled and internally terminated through 50 ohms to AC ground. These modules can operate with CML/LVPECL logic levels. The input signal must have at least a 300mV peak-to-peak differential signal swing. Output from the receiver section of the module is AC coupled CML level and is expected to drive into a 50 ohm load. Different termination strategies may be required depending on the particular chip being interfaced to. **The SPLC-20-P-X-B product family is designed with AC coupled data inputs and outputs to provide the following advantages:**

- Close positioning of Tx/RX chip-set with respect to transceiver; allows for shorter line lengths and at gigabit speeds reduces EMI.
- Minimum number of external components.
- Internal termination reduces the potential for unterminated stubs which would otherwise increase jitter and reduce transmission margin.

Subsequently, this affords the customer the ability to optimally locate the chip-set being interfaced to as close to the SPLC-20-P-X-B as possible and save valuable real estate. At gigabit rates this can provide a significant advantage resulting in better transmission performance and accordingly better signal integrity. Figure 2 illustrates the recommended transmit and receive data lines terminations



	LVPECL Outputs	CML Outputs
R1(Ω)	270 or 130	DNS

Figure 2: Recommended TRANSMIT and RECEIVE Data Terminations

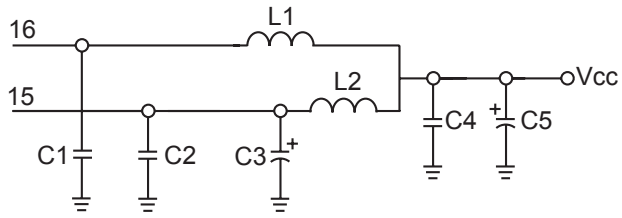
Notes:

A. Consult the Chipset manufacturer's applications information for biasing required for Tx outputs. Some chipset outputs are internally biased and may not need external bias resistors.

B. Consult Chipset manufacturer's data sheet and application data for appropriate receiver input biasing network.

POWER COUPLING

A suggested layout for power and ground connections is given in figure 3 below. Connections are made via separate voltage and ground planes. The ferrite bead should provide an impedance of 220Ω at 100MHz. Bypass capacitors should be placed as close to the 20 pin connector as possible.



VALUES:
C1, C2, C4 = 0.1µF
C3, C5 = 10µF, Tantalum
L1, L2 = Impedance of 220Ω at 100MHz

Figure 3: Suggested Power Coupling

DIGITAL DIAGNOSTIC MONITORING INTERFACE

The SPLC-20-P-X-B modules are provided with internally calibrated digital diagnostic monitoring interface which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage over a 2-wire interface. It also defines a system of alarm flags, which provides users with summary information on whether any of the operating parameters are outside of a factory set normal range. The SPLC-20-P-X-B Digital Diagnostics Monitoring Interface (DDMI) memory map is shown in figure 4 below. The contents of the memory map are described in details on following pages.

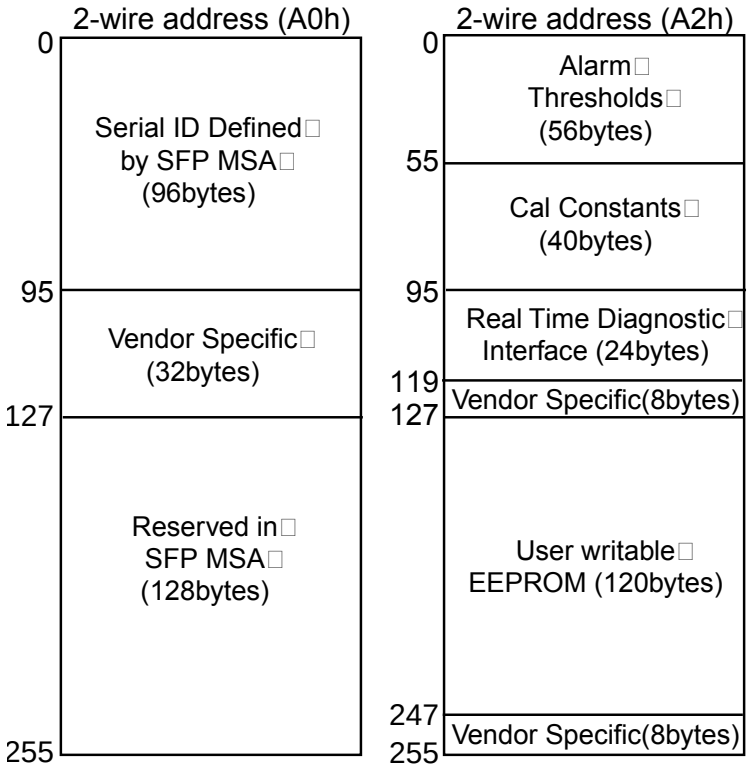


Figure 4: SPLC-20-P-X-B Memory Map

Addr. (DEC)	Hex value	ASCII	Description	Addr (DEC)	Hex value	ASCII	Description	Addr (DEC)	Hex value	ASCII	Description
0	80		Video SFP Transceiver	33	61	a	Vendor name	66	00		BR, Maximum
1	04		SFP function is defined by serial ID only	34	76	v		67	00		BR, Minimum
2	07		LC Connector	35	65	e		68	**XX**		Vendor serial number
3	80		SMPTE 424M/292M/297M/ 259M	36	00		Reserved	69	**XX**		
4	00		Transceiver codes which are not applicable for SMPTE V_SFP transceivers	37	00		Vendor OUI	70	**XX**		
5	00			38	00			71	**XX**		
6	00			39	00			72	**XX**		
7	00			40	53	S	Vendor part number	73	**XX**		
8	00			41	50	P		74	**XX**		
9	00			42	4C	L		75	**XX**		
10	00			43	43	C		76	**XX**		
11	06		SMPTE scrambled	44	2D	-		77	**XX**		
12	1E		BR in 100Mbps	45	32	2		78	**XX**		
13	00		Reserved	46	30	0		79	**XX**		
14	05		Length (9µ) * km	47	2D	-		80	**XX**		
15	32		Length (9µ) * 100m	48	50	P		81	**XX**		
16	00		Length (50µ) * 10m	49	2D	-		82	**XX**		
17	00		Length (62.5µ)*10m	50	32	2		83	**XX**		
18	00		Length (Copper)	51	2D	-		84	**XX**		Vendor date code
19	00		Reserved	52	42	B		85	**XX**		
20	53	S	Vendor name	53	20			86	**XX**		
21	74	t		54	20			87	**XX**		
22	72	r		55	20			88	**XX**		
23	61	a		56	20		Vendor revision	89	**XX**		
24	74	t		57	20			90	**XX**		
25	6F	o		58	20			91	**XX**		
26	73	s		59	20			92	68		Diag. Monitoring type
27	4C	L		60	06		Wavelength = 1550nm	93	F0		Enhanced options
28	69	l		61	0E			94	01		Unspecified
29	67	g		62	00		Reserved	95	**XX**		CC_EXT (64-94)
30	68	h		63	**XX**		CC_BASE (0-62)	96-127	00		Vendor specific
31	74	t		64	00		Options	128-255	00		Reserved
32	77	w		65	1A						

"XX" denotes hex values which varies from module to module.

Table D.1a: EEPROM SERIAL ID MEMORY CONTENTS OF SPLC-20-P-2-B (2-wire address A0h)

Addr. (DEC)	Hex value	ASCII	Description	Addr (DEC)	Hex value	ASCII	Description	Addr (DEC)	Hex value	ASCII	Description
0	80		Video SFP Transceiver	33	61	a	Vendor name	66	00		BR, Maximum
1	04		SFP function is defined by serial ID only	34	76	v		67	00		BR, Minimum
2	07		LC Connector	35	65	e		68	**XX**		Vendor serial number
3	80		SMPTE 424M/292M/297M/ 259M	36	00		Reserved	69	**XX**		
4	00		Transceiver codes which are not applicable for SMPTE V_SFP transceivers	37	00		Vendor OUI	70	**XX**		
5	00			38	00			71	**XX**		
6	00			39	00			72	**XX**		
7	00			40	53	S	Vendor part number	73	**XX**		
8	00			41	50	P		74	**XX**		
9	00			42	4C	L		75	**XX**		
10	00			43	43	C		76	**XX**		
11	06		SMPTE scrambled	44	2D	-		77	**XX**		
12	1E		BR in 100Mbps	45	32	2		78	**XX**		
13	00		Reserved	46	30	0		79	**XX**		
14	23		Length (9µ) * km	47	2D	-		80	**XX**		
15	FF		Length (9µ) * 100m	48	50	P		81	**XX**		
16	00		Length (50µ) * 10m	49	2D	-		82	**XX**		
17	00		Length (62.5µ)*10m	50	32	2		83	**XX**		
18	00		Length (Copper)	51	4D	M		84	**XX**		Vendor date code
19	00		Reserved	52	2D	-		85	**XX**		
20	53	S	Vendor name	53	42	B		86	**XX**		
21	74	t		54	20			87	**XX**		
22	72	r		55	20			88	**XX**		
23	61	a		56	20		Vendor revision	89	**XX**		
24	74	t		57	20			90	**XX**		
25	6F	o		58	20			91	**XX**		
26	73	s		59	20			92	68		Diag. Monitoring type
27	4C	L		60	05		Wavelength = 1310nm	93	F0		Enhanced options
28	69	l		61	1E			94	01		Unspecified
29	67	g		62	00		Reserved	95	**XX**		CC_EXT (64-94)
30	68	h		63	**XX**		CC_BASE (0-62)	96-127	00		Vendor specific
31	74	t		64	00		Options	128-255	00		Reserved
32	77	w		65	1A						

"XX" denotes hex values which varies from module to module.

Table D.1b: EEPROM SERIAL ID MEMORY CONTENTS OF SPLC-20-P-2M-B (2-wire address A0h)

Addr. (DEC)	Hex value	ASCII	Description	Addr (DEC)	Hex value	ASCII	Description	Addr (DEC)	Hex value	ASCII	Description
0	80		Video SFP Transceiver	33	61	a	Vendor name	66	00		BR, Maximum
1	04		SFP function is defined by serial ID only	34	76	v		67	00		BR, Minimum
2	07		LC Connector	35	65	e		68	**XX**		Vendor serial number
3	80		SMPTE 424M/292M/297M/ 259M	36	00		Reserved	69	**XX**		
4	00		Transceiver codes which are not applicable for SMPTE V_SFP transceivers	37	00		Vendor OUI	70	**XX**		
5	00			38	00			71	**XX**		
6	00			39	00			72	**XX**		
7	00			40	53	S	Vendor part number	73	**XX**		
8	00			41	50	P		74	**XX**		
9	00			42	4C	L		75	**XX**		
10	00			43	43	C		76	**XX**		
11	06		SMPTE scrambled	44	2D	-		77	**XX**		
12	1E		BR in 100Mbps	45	32	2		78	**XX**		
13	00		Reserved	46	30	0		79	**XX**		
14	32		Length (9µ) * km	47	2D	-		80	**XX**		
15	FF		Length (9µ) * 100m	48	50	P		81	**XX**		
16	00		Length (50µ) * 10m	49	2D	-		82	**XX**		
17	00		Length (62.5µ)*10m	50	33	3		83	**XX**		
18	00		Length (Copper)	51	2D	-		84	**XX**		Vendor date code
19	00		Reserved	52	42	B		85	**XX**		
20	53	S	Vendor name	53	20			86	**XX**		
21	74	t		54	20			87	**XX**		
22	72	r		55	20			88	**XX**		
23	61	a		56	20		Vendor revision	89	**XX**		
24	74	t		57	20			90	**XX**		
25	6F	o		58	20			91	**XX**		
26	73	s		59	20			92	68		Diag. Monitoring type
27	4C	L		60	06		Wavelength = 1550nm	93	F0		Enhanced options
28	69	l		61	0E			94	01		Unspecified
29	67	g		62	00		Reserved	95	**XX**		CC_EXT (64-94)
30	68	h		63	**XX**		CC_BASE (0-62)	96-127	00		Vendor specific
31	74	t		64	00		Options	128-255	00		Reserved
32	77	w		65	1A						

"XX" denotes hex values which varies from module to module.

Table D.1d: EEPROM SERIAL ID MEMORY CONTENTS OF SPLC-20-P-3-B (2-wire address A0h)

Addr. (DEC)	# of Bytes	Name	Value		
			SPLC-20-P-2	SPLC-20-P-2M	SPLC-20-P-3
00-01	2	Temp High Alarm	+90ºC	+90ºC	+90ºC
02-03	2	Temp Low Alarm	-20ºC	-20ºC	-20ºC
04-05	2	Temp High Warning	+85ºC	+85ºC	+85ºC
06-07	2	Temp Low Warning	-10ºC	-10ºC	-10ºC
08-09	2	Supply Voltage High Alarm	+3.6V	+3.6V	+3.6V
10-11	2	Supply Voltage Low Alarm	+3.0V	+3.0V	+3.0V
12-13	2	Supply Voltage High Warning	+3.47V	+3.47V	+3.47V
14-15	2	Supply Voltage Low Warning	+3.14V	+3.14V	+3.14V
16-17	2	Bias High Alarm	Note C	Note C	Note C
18-19	2	Bias Low Alarm			
20-21	2	Bias High Warning			
22-23	2	Bias Low Warning			
24-25	2	Tx Power High Alarm			
26-27	2	Tx Power Low Alarm			
28-29	2	Tx Power High Warning			
30-31	2	Tx Power Low Warning			
32-33	2	Rx Power High Alarm	0dBm	0dBm	0dBm
34-35	2	Rx Power Low Alarm	-26dBm	-26dBm	-26dBm
36-37	2	Rx Power High Warning	-3dBm	-3dBm	-3dBm
38-39	2	Rx Power Low Warning	-21dBm	-21dBm	-21dBm
40-55	16	Reserved			

Notes C: Varies from module to module

Table D.2: ALARM AND WARNING THRESHOLDS (2-wire address A2h)

Address (DEC)	# Bytes	Name	Description	Value
56-59	4	Rx_PWR (4)	Single precision floating point calibration data, Rx optical Power	0
60-63	4	Rx_PWR (3)		0
64-67	4	Rx_PWR (2)		0
68-71	4	Rx_PWR (1)		1
72-75	4	Rx_PWR (0)		0
76-77	2	Tx_I (Slope)	Fixed decimal (unsigned calibration data, laser bias current	1
78-79	2	Tx_I (Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current	0
80-81	2	Tx_PWR (Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power	1
82-83	2	Tx_PWR (Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power.	0
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature	1
86-87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature.	0
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage.	1
90-91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage.	0
92-94	3	Reserved	Reserved	
95	1	Check Sum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.	

Table D.3: Calibration Constants for Internal Calibration (2-wire address A2h)

Address (DEC)	Bit	Name	Description
96	All	Temperature MSB	Internally measured module temperature
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage (Note D)
99	All	Vcc LSB	
100	All	Tx Bias MSB	Internally measured TX Bias Current (Note E)
101	All	Tx Bias LSB	
102	All	Tx Power MSB	Measured TX output power (Note F)
103	All	Tx Power LSB	
104	All	Rx Power MSB	Measured RX input power (Note G)
105	All	Rx Power LSB	
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input
Optional Status/Control Bits			
110	7	TX Disable state	Digital state of the TX Disable input pin
110	6	Soft TX Disable state	Read/write bit that allows software disable of laser. Writing 1 disables laser.
110	5	Reserved	
110	4	Rx Rate Select State	Not implemented in Video SFP (V_SFP) transceivers
110	3	Soft Rx Rate Select	Not implemented in Video SFP (V_SFP) transceivers
110	2	Tx Fault	Digital state of TX_FAULT
110	1	LOS	Digital state of LOS
110	0	Data_ready_Bar	Indicates V_SFP transceiver has achieved power up and data is ready
111	All	Reserved	

Table D.4: A/D Values and Status Bits (2-wire address A2h)

Notes:

D) The Tx voltage VccT is monitored with accuracy of ±3%

E) The accuracy of bias current measurement is ±10%

F) The accuracy of Tx optical power measurement is ±3dB

G) The accuracy of Rx optical power measurement is ±3dB

Address (DEC)	Bit	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level
	6	Temp Low Alarm	Set when internal temperature is below low alarm level
	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level
	3	Tx Bias High Alarm	Set when Tx Bias current exceeds high alarm level
	2	Tx Bias Low Alarm	Set when Tx Bias current is below low alarm level
	1	Tx Power High Alarm	Set when Tx output power exceeds high alarm level
	0	Tx Power Low Alarm	Set when Tx output power is below low alarm level
113	7	Rx Power High Alarm	Set when Received power exceeds high alarm level
	6	Rx Power Low Alarm	Set when Received power is below low alarm level
	5-0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level
	6	Temp Low Warning	Set when internal temperature is below low warning level
	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level
	4	Vcc Low Warning	Set when internal supply voltage is below low warning level
	3	Tx Bias High Warning	Set when Tx Bias current exceeds high warning level
	2	Tx Bias Low Warning	Set when Tx Bias current is below low warning level
	1	Tx Power High Warning	Set when Tx output power exceeds high warning level
	0	Tx Power Low Warning	Set when Tx output power is below low warning level
117	7	Rx Power High Warning	Set when Received power exceeds high warning level
	6	Rx Power Low Warning	Set when Received power is below low warning level
	5-0	Reserved Warning	
118	7-0	Reserved	
119	7-0	Reserved	

Table D.5: Alarm and Warning Flags (2-wire address A2h)

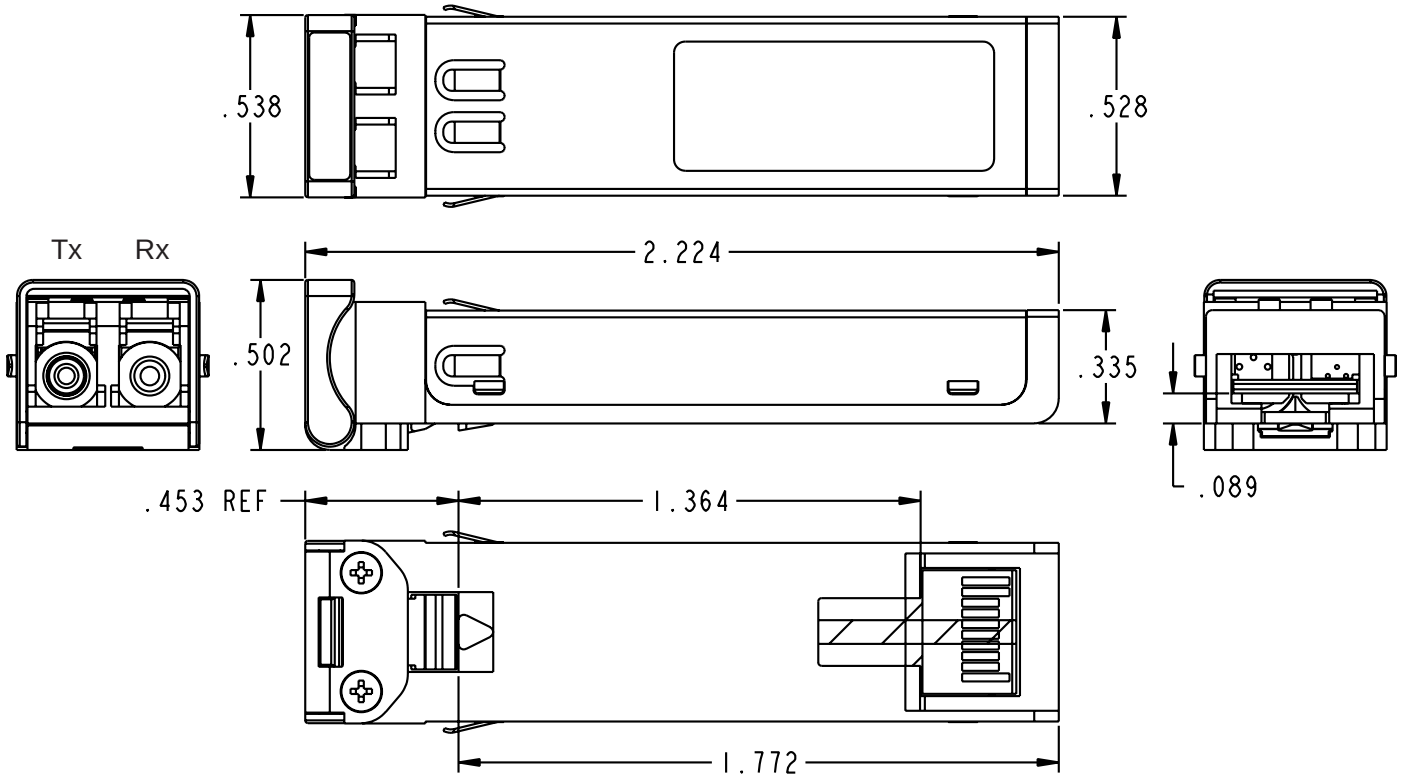
Address (DEC)	# Bytes	Name	Description
120-127	8	Vendor Specific	Vendor Specific

Table D.6: Vendor Specific Memory Addresses (2-wire address A2h)

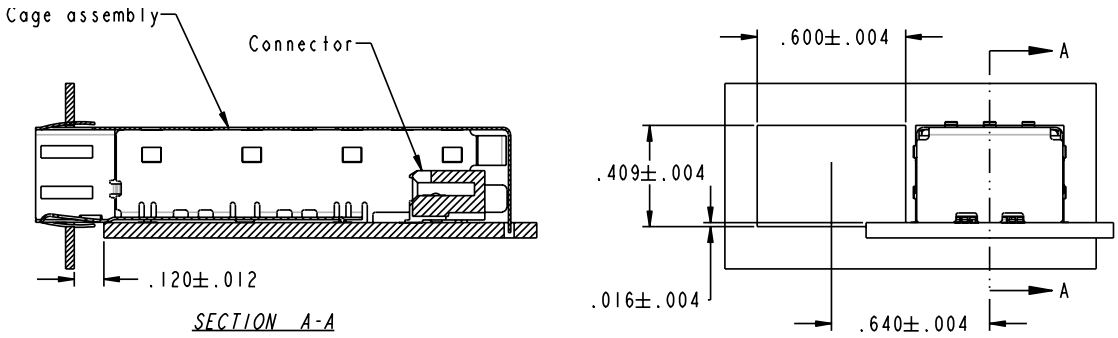
Address (DEC)	# Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM
248-255	8	Vendor Specific	Vendor specific control functions

Table D.7: User EEPROM (2-wire address A2h)

V_SFP TRANSCEIVER MECHANICAL DIMENSIONS (inches)

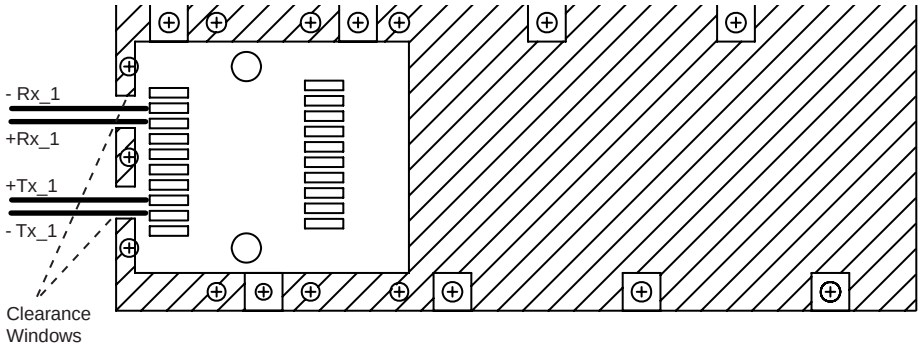


V_SFP PANEL CUTOUT

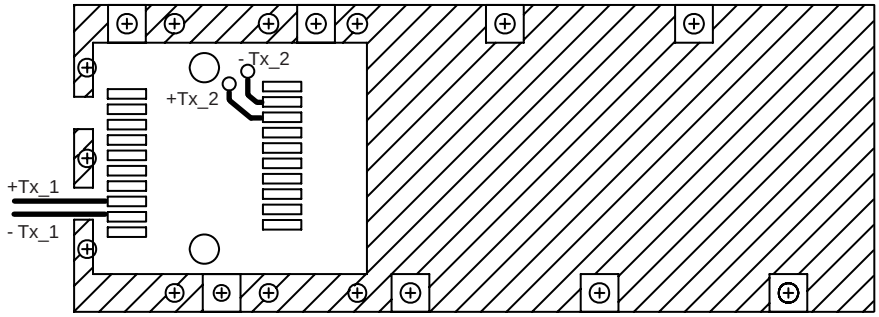


VIDEO SFP RECOMMNEDED HOST LAYOUT:

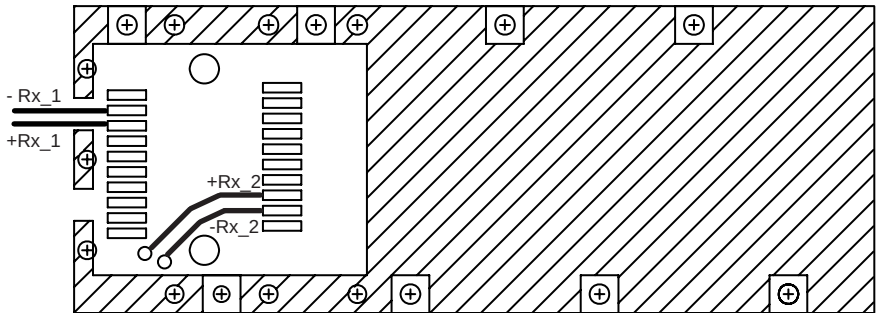
The video transceiver, dual transmitter, dual receiver, simplex transmitter, and simplex receiver modules share identical signal pin-outs. This provides the host flexibility to design one PCB to accommodate all three video SFPs. The video cage, however has only two signal trace clearance windows. Therefore, we recommend routing ±TX_2 and ±RX_2 signal traces to the bottom PCB layer before crossing through the video SFP cage outline.



Video SFP Transceiver(Tx/Rx)
NOTE: ±TX_2 AND ±RX_2 are not internally connected in Video SFP transceiver



Dual Transmitter Video SFP (Tx/Tx)
NOTE: ±TX_2 are not internally connected in simplex transmitter Video SFP



Dual Receiver Video SFP (Rx/Rx)
NOTE: ±RX_2 are not internally connected in simplex receiver Video SFP

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