

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics



ORDERING INFORMATION

SP2R-20-9D - 2 - B

RELEASE ACTUATOR

B = Bail Actuator

RECEIVER TYPE

2 = Long Wavelength Dual PIN RX

COMMUNICATIONS PROTOCOL

9D = SMPTE 292M/297M/259M
with Digital Diagnostics;
143MBaud to 1.485GBaud



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Features

- SMPTE 292M/297M/259M compatible
- Based on industry standard SFP
- Handles Pathological test pattern
- Internally calibrated Digital Diagnostic Monitoring Interface
- RoHS-6 compliant
- 100Ω differential AC coupled CML level Outputs
- Die Cast Metal Housing
- Hot pluggable
- Single +3.3V Power Supply

PRODUCT OVERVIEW

The SP2R-20-9D-2-B Video Small form Factor Pluggable (V_SFP) optical dual receiver modules are high performance integrated duplex data links for unidirectional communication over single mode optical fiber. The SP2R-25-9 transceivers are designed to receive data rates from 143Mbps to 1.485Gbps and are compatible with the following standards:

- SMPTE 297M/292M (HDTV -- 1.485Gbps)
- SMPTE 297M/259M (SDTV -- 143/177/270/360Mbps)

The Stratos Lightwave dual receiver V_SFP module is hot pluggable which allows a suitably designed enclosure to be changed from one type of external interface to another simply by plugging in a V_SFP having the alternative external interface. The SP2R-20-9D-2-B operates using a single 3.3V supply.

This optoelectronic dual receiver module is designed to operate with a transmitter that is Class 1 Laser product compliant with FDA Radiation Performance Standards, 21 CFR Subchapter J and International Safety Standard IEC-825-1.

LONG WAVELENGTH RECEIVER

The SP2R-20-9D-2-B is provided with single mode PIN pre-amp subassemblies with angle polished fiber stub.

MODULE SPECIFICATIONS - ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	Tstg	-40	+85	°C	
Supply Voltage	V _{CC} T, V _{CC} R		6.0	V	VCC - ground
Data AC Voltage	Tx+, Tx-		2.6	V _{pp}	Differential
Data DC Voltage	Tx+, Tx-	-10	10	V _{pk}	V(Tx+ or Tx-) - ground

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MODULE SPECIFICATION - RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Ambient Case Temperature	Tc	0		+70	°C	
Supply Voltage	V _{DDT} , V _{DDR}	+3.135	+3.3	+3.435	VDC	
Baud Rate	BRate	143		1485	MBaud	143/177/270/360/1485MBaud

PERFORMANCE SPECIFICATIONS - ELECTRICAL

0°C<Tc<+70°C; +3.135<Vcc<+3.465V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc		160	200	mA	Tc = 25°C, Vcc = +3.3 V
				300	mA	0°C<Tc<+70°C, +3.135 V< Vcc <+3.465V
Surge Current	I _{surge}			30	mA	Surge above steady state value
CML Outputs (Differential)		400	800	1200	mVpp	AC Coupled Outputs
Total Jitter [Pk - Pk]	TJ			135	ps	Measured with Color Bar Test Signal @1.485Gbps (note 1)
				740	ps	Measured with Color Bar Test Signal @143/177/270/360Mbps
Return Loss		15			dB	Worst case @ 10KHz to 3GHz
SCL, SDA	VoH	2.5		Vcc+0.3	V	
	VoL	0		0.5	V	

SP2R-20-9D-2-B OPTICAL SPECIFICATIONS - Dual PIN RX

0°C<Tc<+70°C; +3.135<Vcc<+3.465V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
LINK DISTNACE						
9.0µm Core Diameter SMF (note2)		10			km	1.485Gbps
		15			km	143/177/270/360Mbps
RECEIVER						
Optical Input Wavelength	λ	1270		1610	nm	
Optical Input Power	Pr	-20		-1	dBm	Note 3
Optical Return Loss	ORL	29			dB	
RX_LOS --- Asserted	Pa	-29			dBm	No Signal Pins Designated for RX_LOS. Assert/Deassert Levels can be Monitored via Digital Diagnostics Interface.
RX_LOS --- Deasserted	Pd			-20	dBm	
RX_LOS --- Hysteresis	Pa - Pd		1.5	5	dB	

Note 1: Maximum Jitter is specified for single module point-to-point applications only. In cascaded configurations, where the receiver electrical output is directly interfaced with the transmitter electrical input of a separate module, accumulated jitter may result in CRC errors to occur during pathological pattern transmission. For error-free operation in such a situation, use of re-clocker device is recommended at the output of the receiver before interfacing to the inputs of the optical transmitter. This will ensure that the output jitter will not exceed the input jitter tolerance of the succeeding transmitter input.

Note 2: The specified minimum link distances are based on IEEE link budget models. Assumes minimum transmitter output power and extinction ratio (SP2T-20-9D-2-B) and worst case receiver sensitivity with color bar test signal at 140/177/270/360/1485Mbps. The minimum link distances will be reduced with SDI test matrix. Please contact factory to discuss specific applications.

Note 3: Minimum receiver input power is defined for line BER < 1 x 10⁻¹⁰ running PRBS 2²³ - 1 at 140/177/270/360/1485Mbps

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

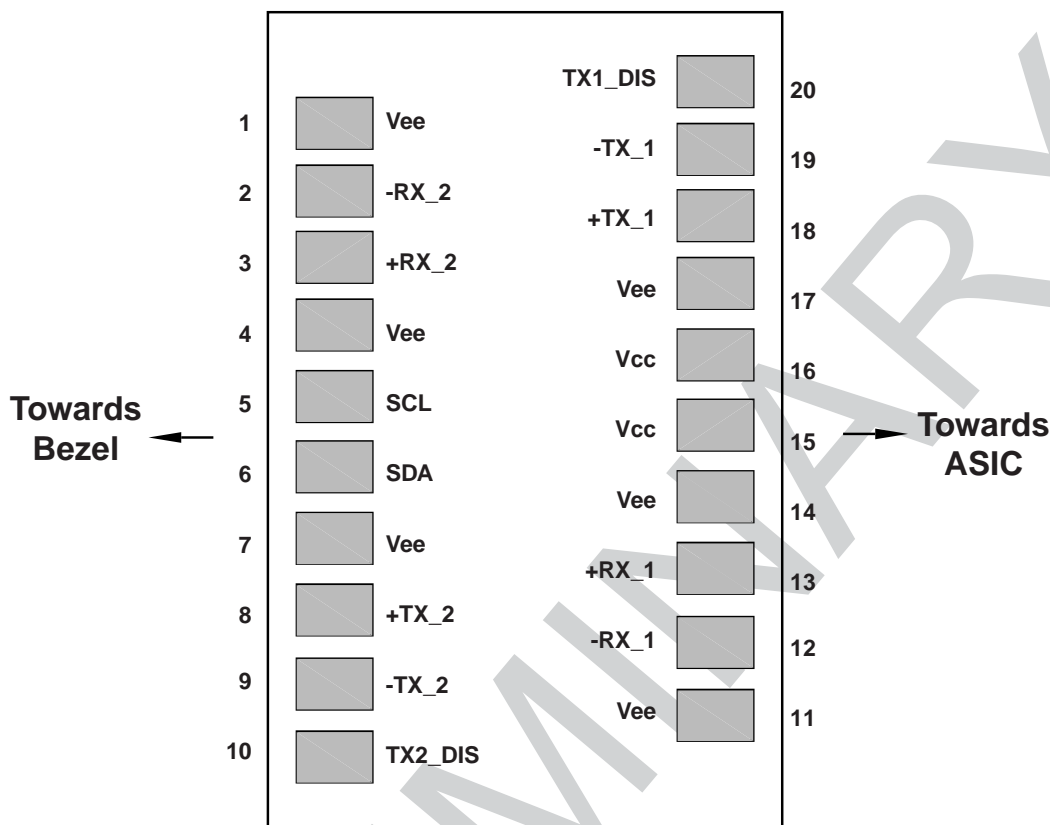


Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names

PIN NO.	NAME	FUNCTION	PLUG SEQ.	NOTES
PIN 1	Vee	Signal Ground	1	
PIN 2	-RX_2	Inverted Received Data out (2)	3	Note 4
PIN 3	+RX_2	Non-Inverted Received Data out (2)	3	Note 4
PIN 4	Vee	Signal Ground	1	
PIN 5	SCL	Serial Clock	3	
PIN 6	SDA	Serial Data	3	
PIN 7	Vee	Signal Ground	1	
PIN 8	+TX_2	Non-inverted Data In (2)	3	Note 5
PIN 9	-TX_2	Inverted Data In (2)	3	Note 5
PIN 10	TX2_DIS	Transmitter Disable (2)	3	Note 6
PIN 11	Vee	Signal Ground	1	
PIN 12	-RX_1	Inverted Received Data out	3	Note 4
PIN 13	+RX_1	Non-Inverted Received Data out	3	Note 4
PIN 14	Vee	Signal Ground	1	
PIN 15	Vcc	Power Supply	2	+3.3V ±5%, Note 7
PIN 16	Vcc	Power Supply	2	+3.3V ±5%, Note 7
PIN 17	Vee	Signal Ground	1	
PIN 18	+TX_1	Non-inverted Data In	3	Note 5
PIN 19	-TX_1	Inverted Data In	3	Note 5
PIN 20	TX1_DIS	Transmitter Disable	3	Note 6

Plug Sequence: Pin engagement sequence during hot plugging.

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NOTES:

(4) \pm RX_1 and \pm RX_2: These are the differential receiver CML level outputs. They are AC coupled 100ohm differential lines which should be terminated with 100ohm (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 1200mV differential (200-600mV single ended) when properly terminated. Refer to figure 2, 3, 4 for recommended receive data lines terminations.

(5) \pm TX_1 and \pm TX_2: Floating; Not internally connected

(5) TX1_DIS and TX2_DIS: Floating; Not Internally Connected.

(6) Vcc: are the receiver and transmitter power supplies. They are defined as 3.3V \pm 5% at the V_SFP connector pin. Maximum supply current is 360mA. Recommended host board power supply filtering is shown in figure 3. When the recommended supply filtering network is used, hot plugging of the V_SFP module will result in an inrush current of no more than 30mA greater than the steady state value.

TERMINATION CIRCUITS

Output from the SP2R-20-9D-2-B dual receiver module is AC coupled CML level and is expected to drive into a 50 ohm load. Different termination strategies may be required depending on the particular chip being interfaced to. **The SP2R-20-9D-2-B product family is designed with AC coupled data outputs to provide the following advantages:**

- Close positioning of receiver chip-set with respect to SP2R-20-9D-2-B; allows for shorter line lengths and at gigabit speeds reduces EMI.
- Minimum number of external components.
- Internal termination reduces the potential for unterminated stubs which would otherwise increase jitter and reduce transmission margin.

Subsequently, this affords the customer the ability to optimally locate the chip-set being interfaced to as close to the SP2R-20-9D-2-B as possible and save valuable real estate. At gigabit rates this can provide a significant advantage resulting in better transmission performance and accordingly better signal integrity. Figure 2 on following page illustrates the recommended receive data line terminations.

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

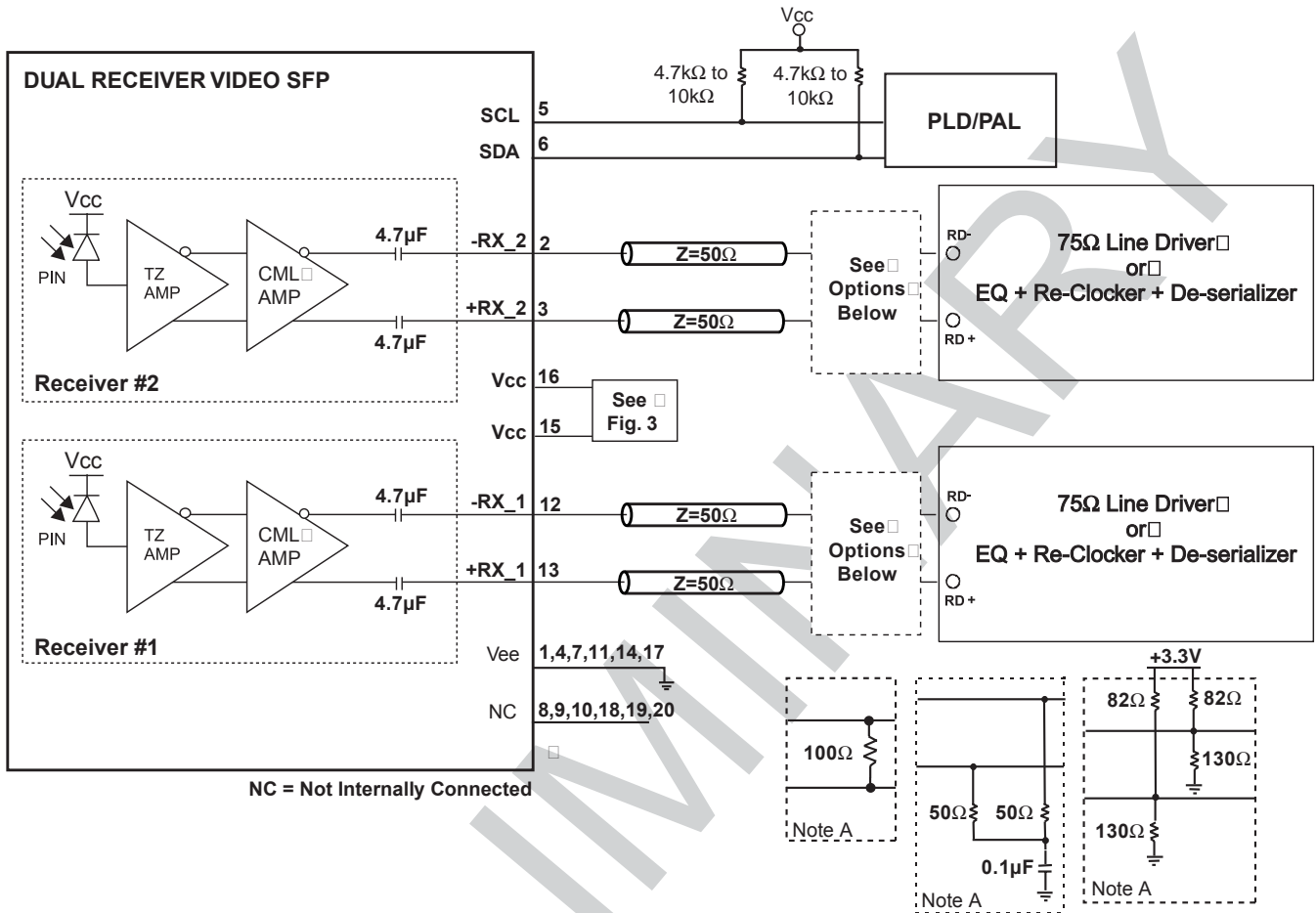
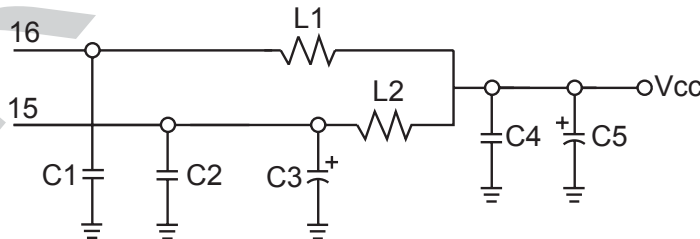


Figure 2. Recommended RECEIVE Data Lines Terminations

Note A: Consult Chipset manufacturer's data sheet and application data for appropriate receiver input biasing network.

POWER COUPLING

A suggested layout for power and ground connections is given in figure 3 below. Connections are made via separate voltage and ground planes. The ferrite bead should provide an impedance of 220Ω at 100MHz. Bypass capacitors should be placed as close to the 20 pin connector as possible.



VALUES: □

C1, C2, C4 = 0.1µF □

C3, C5 = 10µF, Tantalum □

L1, L2 = Impedance of 220Ω at 100MHz

Figure 3. Suggested Power Coupling

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

DIGITAL DIAGNOSTIC MONITORING INTERFACE

The SP2R-9D-2-B dual receiver modules are provided with internally calibrated digital diagnostic monitoring interface which allows real-time access to device operating parameters such as module temperature, received optical power and module supply voltage over a 2-wire interface. It also defines a system of alarm flags, which provides users with summary information on whether any of the operating parameters are outside of a factory set normal range.

The SP2R-9D-2-B dual receiver SFP module is designed with two memory devices (one for each receiver). The Digital Diagnostics Monitoring Interface (DDMI) memory map is shown in figure 4 below. The contents of the memory map are described in details on following pages.

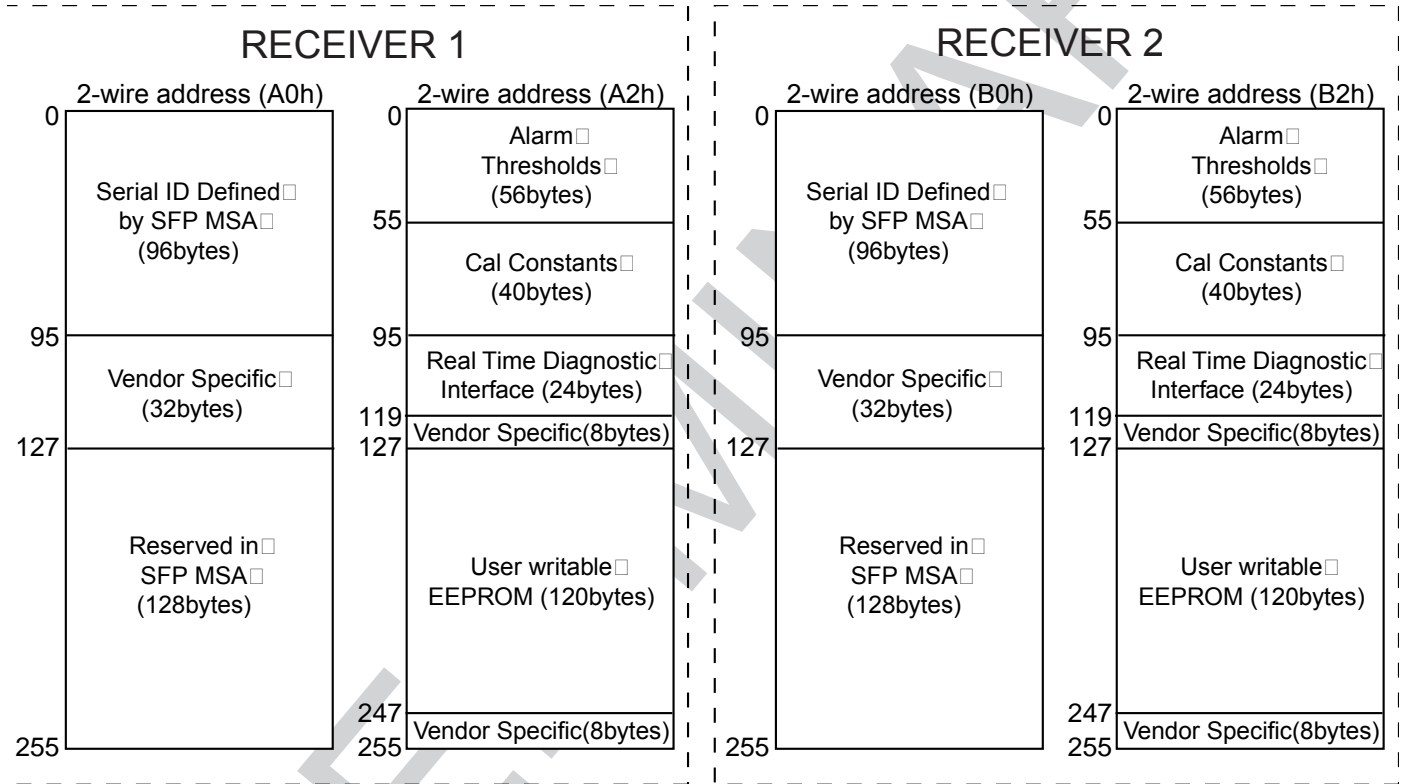


Figure 4. SP2R-20-9D-2-B (Dual Receiver V_SFP) Memory Map

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

Addr. (DEC)	Hex Value	ASCII	Description	Addr. (DEC)	Hex value	ASCII	Description	Addr. (DEC)	Hex value	ASCII	Description
0	82		Dual Receiver Video SFP (V_SFP)	33	61	a	Vendor name (cont)	66	00		Max. and Min. bit rate -- Unspecified
1	04		SFP function is defined by serial ID only	34	76	v		67	00		
2	07		LC Connector	35	65	e		68			Vendor serial number
3	40		SMPTE 292M/297/259M	36	00		Reserved	69			
4	00		Transceiver codes which are not applicable for SMPTE SFP transceivers	37	00		Vendor OUI -- Unspecified	70			
5	00			38	00			71			
6	00			39	00			72			
7	00			40	53	S	73				
8	00			41	50	P	74				
9	00			42	32	2	75				
10	00			43	52	R	76				
11	06		SMPTE scrambled	44	2D	-	Vendor part number	77			
12	0F		Nominal bit rate in units of 100Mb/s	45	32	2		78			
13	00		Reserved	46	30	0		79			
14	0A		Length (9μ)*km	47	2D	-		80			
15	64		Length (9μm)*100m	48	39	9		81			
16	00		Length (50μm)	49	44	D		82			
17	00		Length (62.5μm)	50	2D	-		83			
18	00		Length (Copper)	51	32	2		84			
19	00		Reserved	52	2D	-		85			
20	53	S	Vendor name	53	42	B		Vendor revision	86		
21	74	t		54	20		87				
22	72	r		55	20		88				
23	61	a		56	2		89				
24	74	t		57	20		90				
25	6F	o		58	20		91				
26	73	s		59	20		92	68		Internally Calibrated and Rx power type = Avg. Power	
27	4C	L		Vendor name	60	05		Single Mode Receivers	93	90	
28	69	l	61		1E		Reserved	94	01		Unspecified
29	67	g	62		00			95	XX		CC_EXT (64-94)
30	68	h	63		XX		CC_BASE (0-62)	96-127	00		Vendor specific
31	74	t	64		00		Option values	128-255	00		Reserved
32	77	w	65		02						

Table D.1: Serial ID Data Files (2-wire Address A0h & B0h)

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

Address (DEC)	# Bytes	Name	Description	Value
00-01	2	Temp High Alarm	MSB at low address	+90°C
02-03	2	Temp Low Alarm	MSB at low address	-20°C
04-05	2	Temp High Warning	MSB at low address	+85°C
06-07	2	Temp Low Warning	MSB at low address	-10°C
08-09	2	Supply Voltage High Alarm	MSB at low address	+3.6V
10-11	2	Supply Voltage Low Alarm	MSB at low address	+3.0V
12-13	2	Supply Voltage High Warning	MSB at low address	+3.47V
14-15	2	Supply Voltage Low Warning	MSB at low address	+3.14V
16-17	2	Bias High Alarm	MSB at low address	N/A
18-19	2	Bias Low Alarm	MSB at low address	N/A
20-21	2	Bias High Warning	MSB at low address	N/A
22-23	2	Bias Low Warning	MSB at low address	N/A
24-25	2	Tx Power High Alarm	MSB at low address	N/A
26-27	2	Tx Power Low Alarm	MSB at low address	N/A
28-29	2	Tx Power High Warning	MSB at low address	N/A
30-31	2	Tx Power Low Warning	MSB at low address	N/A
32-33	2	Rx Power High Alarm	MSB at low address	0dBm
34-35	2	Rx Power Low Alarm	MSB at low address	-40dBm
36-37	2	Rx Power High Warning	MSB at low address	-3dBm
38-39	2	Rx Power Low Warning	MSB at low address	-30dBm
40-55	16	Reserved	Reserved for future monitored quantities	

Table D.2: ALARM AND WARNING THRESHOLDS (2-wire address A2h & B2h)

Address (DEC)	# Bytes	Name	Description	Value
56-59	4	Rx_PWR (4)	Single precision floating point calibration data, Rx optical Power	0
60-63	4	Rx_PWR (3)		0
64-67	4	Rx_PWR (2)		0
68-71	4	Rx_PWR (1)		1
72-75	4	Rx_PWR (0)		0
76-77	2	Tx_I (Slope)	Not applicable for dual receiver video SFP module	
78-79	2	Tx_I (Offset)	Not applicable for dual receiver video SFP module	
80-81	2	Tx_PWR (Slope)	Not applicable for dual receiver video SFP module	
82-83	2	Tx_PWR (Offset)	Not applicable for dual receiver video SFP module	
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature	1
86-87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature.	0
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage.	1
90-91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage.	0
92-94	3	Reserved	Reserved	
95	1	Check Sum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.	

**Table D.3: CALIBRATION CONSTANTS FOR INTERNALLY CALIBRATED V_SFP
(2-wire address A2h & B2h)**

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

Address (DEC)	Bit	Name	Description
96	All	Temperature MSB	Internally measured module temperature
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage (Note A)
99	All	Vcc LSB	
100	All	TxBias MSB	Not Applicable for dual receiver video SFP module
101	All	TxBias LSB	
102	All	TxPower MSB	Not Applicable for dual receiver video SFP module
103	All	TxPower LSB	
104	All	RxPower MSB	Measured RX input power (Note B)
105	All	RxPower LSB	
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input
Optional Status/Control Bits			
110	7	TX Disable state	Not Applicable for dual receiver video SFP module
110	6	Soft TX Disable state	Not Applicable for dual receiver video SFP module
110	5	Reserved	
110	4	Rx Rate Select State	Not implemented in dual receiver Video SFP
110	3	Soft Rx Rate Select	Not implemented in dual receiver Video SFP
110	2	TxFault	Not Applicable for dual receiver video SFP module
110	1	LOS	Digital state of the LOS
110	0	Data_ready_Bar	Indicates Video SFP has achieved power up and data is ready
111	All	Reserved	

Table D.4: A/D Values and Status Bits (2-wire address A2h & B2h)

Note A: The Tx voltage VccT is monitored with accuracy of $\pm 3\%$

Note B: The accuracy of Rx optical power measurement is $\pm 3\text{dB}$

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

ALARM FLAGS:

Data address 112-119 (Table D.5) contain an optional set of alarm bits. These alarm flags are not latched. It is recommended that the detection of an asserted flag bit should be verified by a second read of the flag at least 100msec later. For users who do not wish to set their own threshold values (address 0 to 55 at 2-wire address A0h & B0h) or read the values (address 0 - 55 at 2-wire address A2h & B2h), the flags alone can be monitored.

Data Address	Bits	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceed high alarm level
	6	Temp Low Alarm	Set when internal temperature is below low alarm level
	5	Vcc High Alarm	Set when internal supply voltage exceed high alarm level
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level
	3	TX Bias High Alarm	Not applicable for dual receiver video SFP module
	2	TX Bias Low Alarm	
	1	TX Power High Alarm	
	0	TX Power Low Alarm	
113	7	RX Power High Alarm	Set when internal RX input power exceed high alarm level
	6	RX Power Low Alarm	Set when internal RX input power is below low alarm level
	5	Reserved Alarm	
	4	Reserved Alarm	
	3	Reserved Alarm	
	2	Reserved Alarm	
	1	Reserved Alarm	
	0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceed high Warning level
	6	Temp Low Warning	Set when internal temperature is below low Warning level
	5	Vcc High Warning	Set when internal supply voltage exceed high Warning level
	4	Vcc Low Warning	Set when internal supply voltage is below low Warning level
	3	TX Bias High Warning	Not applicable for dual receiver video SFP module
	2	TX Bias Low Warning	
	1	TX Power High Warning	
	0	TX Power Low Warning	
117	7	RX Power High Warning	Set when internal RX input power exceed high Warning level
	6	RX Power Low Warning	Set when internal RX input power is below low Warning level
	5	Reserved Warning	
	4	Reserved Warning	
	3	Reserved Warning	
	2	Reserved Warning	
	1	Reserved Warning	
	0	Reserved Warning	
118	All	Reserved	
119	All	Reserved	

Table D.5: Alarm Flag Bits (2-wire Address A2h & B2h)

Data Address	# Bytes	Name	Description
120-127	All	Vendor Specific	Vendor Specific

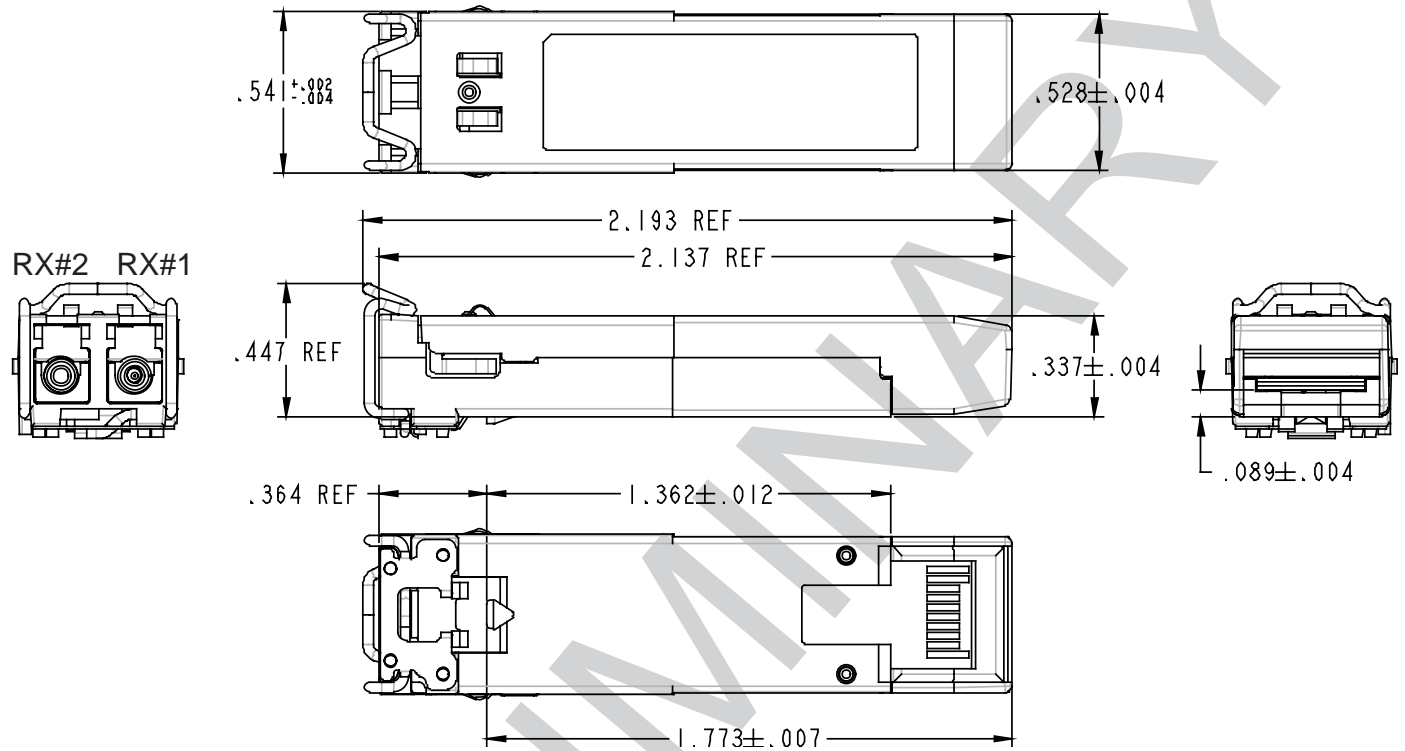
Table D.6: Vendor Specific Memory Addresses (2-wire Address A2h & B2h)

Data Address	# Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM
248-255	8	Vendor Specific	Vendor specific control functions

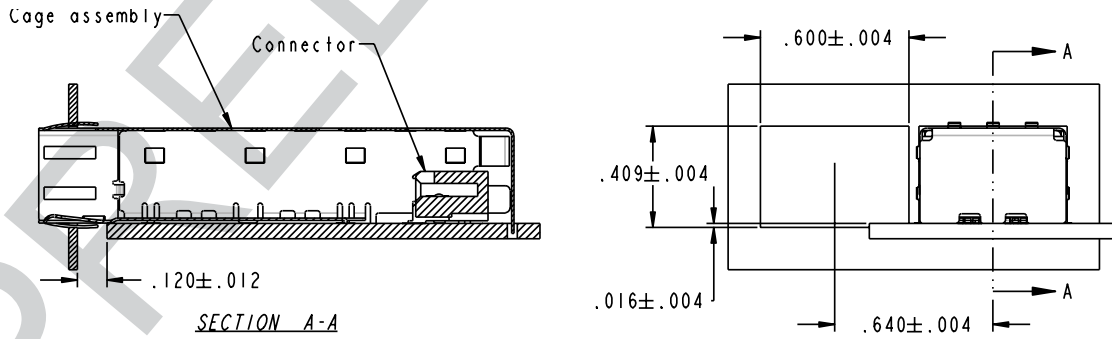
Table D.7: User Accessible EEPROM (2-wire Address A2h & B2h)

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

V_SFP MECHANICAL DIMENSIONS (inches) with BAIL ACTUATOR



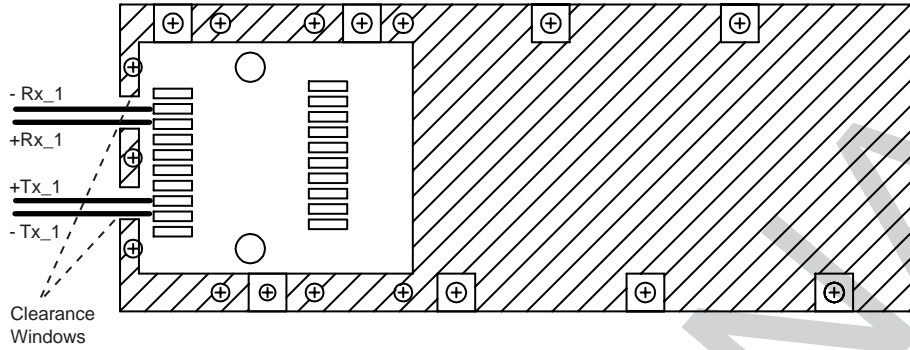
V_SFP PANEL CUTOUT



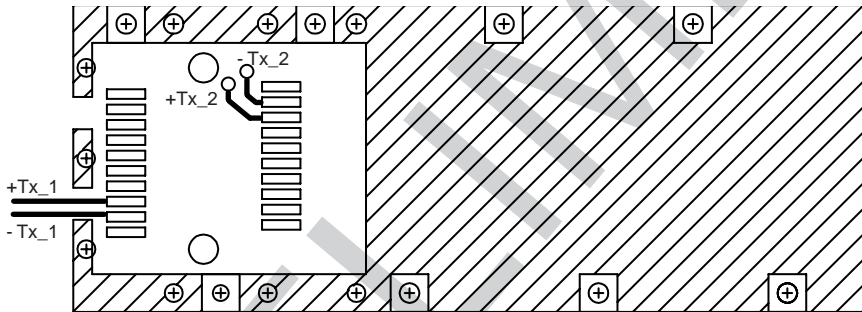
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VIDEO SFP RECOMMENDED HOST LAYOUT:

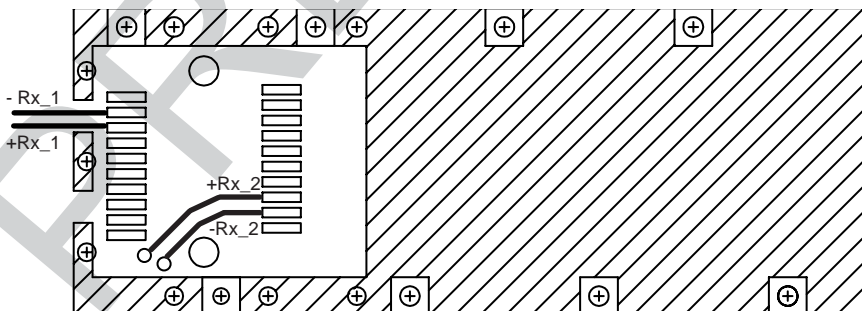
The video transceiver, dual transmitter, dual receiver, simplex transmitter, and simplex receiver modules share identical signal pin-outs. This provides the host flexibility to design one PCB to accommodate all three video SFPs. The video cage, however has only two signal trace clearance windows. Therefore, we recommend routing $\pm TX_2$ and $\pm RX_2$ signal traces to the bottom PCB layer before crossing through the video SFP cage outline.



**Video SFP Transceiver
SPLC-20-9D-X-X (TX/RX)**
**NOTE: $\pm TX_2$ AND $\pm RX_2$
are not internally con-
nected in Video SFP
transceiver**



**Dual Transmitter Video SFP
SP2T-20-9D-X-X (TX/TX)**
**NOTE: $\pm TX_2$ are not
internally connected in
simplex transmitter Video
SFP (SP1T-20-9D-X-B)**



**Dual Receiver Video SFP
SP2R-20-9D-X-X (RX/RX)**
**NOTE: $\pm RX_2$ are not
internally connected in
simplex receiver Video
SFP (SP1R-20-9D-X-X)**

SP2R-20-9D-2-B Optical SMPTE 292M/297M/259M Dual Receiver Video SFP (V_SFP) w/ Digital Diagnostics

STRATOS

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